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Semicon 2.0: India Semiconductor Mission Enters Its Second Phase

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SCIENCE & TECH

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WHY IN NEWS

On **July 15, 2026**, the Union Cabinet approved **Semicon 2.0**, the second phase of the **India Semiconductor Mission (ISM)**, with a total outlay of **Rs 1,27,500 crore**. Building on **ISM 1.0**, the mission aims to make India a global hub across the entire semiconductor value chain, from chip design to advanced fabrication and packaging.

FROM ISM 1.0 TO SEMICON 2.0

India's semiconductor push began with the **India Semiconductor Mission (ISM)** launched under the **Ministry of Electronics and Information Technology (MeitY)**. **ISM 1.0** attracted the country's first commercial fabrication and assembly investments, of which the flagship is the **Micron facility at Sanand, Gujarat**. **Semicon 2.0** now widens the scope from a small set of anchor projects to a **whole-of-ecosystem** strategy, with the first advanced fabs targeted for commissioning around **2028**.

The strategic logic is **semiconductor sovereignty** (<https://ujjyari.com/vocab/sovereignty/>). Chips power everything from smartphones and cars to missiles and satellites, yet global manufacturing is concentrated in a handful of geographies. The COVID-era chip shortage exposed the fragility of these supply chains. **Semicon 2.0** is therefore framed as part of **Atmanirbhar Bharat**, supply-chain **resilience** (<https://ujjyari.com/vocab/resilience/>), and the **China+1 / friend-shoring** realignment in which democracies seek trusted alternative suppliers.

The Six Pillars of Semicon 2.0

The mission is organised around a value-chain approach rather than a single product. Each pillar targets one link in the chain so that gaps do not force continued import dependence.

PILLAR	FOCUS AREA	WHAT IT COVERS
1	Chip design	EDA tools, design startups, IP cores
2	Machinery and materials	Fab equipment, gases, chemicals, wafers
3	New fabs	Silicon, compound, display and discrete-device fabs
4	ATMP / OSAT	Assembly, packaging and testing capacity
5	R&D and nodes	Moving from 28nm-110nm toward advanced nodes
6	Talent	Skilling engineers and researchers at scale

Key Terms Decoded

A few technical terms recur in every semiconductor discussion and are high-value for Prelims:

- **ATMP = Assembly, Testing, Marking and Packaging**, the back-end stage that turns a fabricated wafer into a usable, protected chip.
- **OSAT = Outsourced Semiconductor Assembly and Test**, third-party firms that provide ATMP services to fabless companies.
- **Node** = the **transistor gate length**, measured in nanometres. A smaller node (for example 5nm versus 28nm) means more transistors, higher performance and lower power use.

Ecosystem Built So Far

The design and talent base is already taking shape. India now hosts about **105 chip-design startups**, and roughly **68,000 students have been trained across 315 universities** on industry-standard **EDA (Electronic Design Automation)** tools. This design-led strength plays to India's existing engineering talent pool even as physical fabs take years to mature.

The Challenges Ahead

Fabrication is one of the most capital-intensive industries on earth. A single advanced fab can cost billions of dollars and takes years to break even, so **fab economics** remain daunting. Fabs are also **water and power intensive**, demanding ultra-pure water and uninterrupted electricity, which strains local resources. Finally, the **skilled-talent gap** in fabrication and process engineering, as distinct from design, must be closed for the mission to succeed.

UPSC RELEVANCE

GS Paper 3: Indian economy, science and technology, [indigenisation](https://ujiyari.com/vocab/indigenisation/) (https://ujiyari.com/vocab/indigenisation/) of technology, and developing new technology. Semiconductor policy links industrial policy, strategic autonomy and supply-chain security.

Prelims pointers:

- ISM is implemented under **MeitY**.
- Semicon 2.0 outlay: **Rs 1,27,500 crore** (approved July 15, 2026).
- First commercial fab under ISM 1.0: **Micron, Sanand, Gujarat**.
- ATMP** and **OSAT** full forms and their back-end role.
- “Node” refers to **transistor gate length** in nanometres.

Mains question: “Semiconductor self-reliance is as much about **geopolitics** (<https://ujiyari.com/vocab/geopolitics/>) as it is about technology.” Analyse how India’s Semicon 2.0 mission addresses both dimensions, and identify the key structural challenges to achieving it.

FACTS CORNER

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Parent programme: India Semiconductor Mission (ISM), under MeitY.

Semicon 2.0 outlay: Rs 1,27,500 crore, approved by the Union Cabinet on July 15, 2026.

Six pillars: chip design; machinery and materials; new fabs; ATMP/OSAT; R&D and advanced nodes; talent development.

Anchor project (ISM 1.0): Micron ATMP unit at Sanand, Gujarat.

First advanced fabs: targeted for commissioning around 2028.

Ecosystem: ~105 chip-design startups; ~68,000 students trained across 315 universities.

Strategic frame: semiconductor sovereignty, China+1 / friend-shoring, Atmanirbhar Bharat.

Sources: *PIB* (<https://pib.gov.in/>), *MeitY India Semiconductor Mission* (<https://www.meity.gov.in/>), *The Hindu* (<https://www.thehindu.com/>), *Indian Express* (<https://indianexpress.com/>)

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