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3D Glass Semiconductor Packaging — India's First Facility at Bhubaneswar

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3D Glass Semiconductor Packaging — India's First Facility at Bhubaneswar

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WHY IN NEWS

India's **first 3D glass chip packaging facility** has been established in **Bhubaneswar, Odisha**, marking a significant step in India's semiconductor ambitions. The facility uses **glass substrates** — replacing conventional silicon and organic materials — to enable **through-glass vias (TGVs)** for vertical signal transfer between stacked chips. With a target capacity of **70,000 panels and 50 million units annually**, the project aligns with the **India Semiconductor Mission (ISM)** under which the government has committed **₹76,000 crore** to build domestic semiconductor manufacturing and packaging capacity. The technology addresses the limits of traditional chip scaling and is critical for **AI accelerators and defence electronics**.

THE SEMICONDUCTOR PACKAGING REVOLUTION

Why Packaging Matters

For decades, semiconductor progress followed **Moore's Law** — the observation by Intel co-founder Gordon Moore that transistor density on chips doubles approximately every two years. But Moore's Law is approaching physical limits:

- Transistors are now measured in **angstroms** (sub-2nm nodes)
- Further miniaturisation faces **quantum tunnelling leakage**, heat dissipation walls, and exponentially rising fabrication costs

The industry's response is **advanced packaging** — instead of making individual chips smaller, stack multiple specialised chips together in a single package that behaves like one powerful chip.

Types of Advanced Packaging

TECHNOLOGY	DESCRIPTION	KEY PLAYERS
2.5D packaging	Chips side-by-side on a silicon interposer	TSMC CoWoS, Intel EMIB
3D packaging	Chips stacked vertically with direct connections	TSMC SoIC, Samsung X-Cube
Fan-Out Wafer Level Packaging (FOWLP)	Chips embedded in reconstituted wafer	TSMC InFO
Chiplets	Disaggregated chips combined in one package	Intel Tile architecture, AMD
Glass substrate packaging	Glass replaces organic PCB substrate	Intel, India Bhubaneswar facility

GLASS SUBSTRATE TECHNOLOGY — THE INNOVATION

What Is a Glass Substrate?

In semiconductor packaging, a **substrate** is the base layer that:

- Provides **electrical connections** between the chip and the circuit board
- Carries **power and signals** to and from the chip
- Provides **structural support**

Traditional substrates use **organic materials** (fibreglass-reinforced polymer laminates — similar to PCBs) or **silicon interposers**. Both have limitations:

PARAMETER	ORGANIC SUBSTRATE	SILICON INTERPOSER	GLASS SUBSTRATE
Signal loss	Higher	Lower	**Lowest**
Thermal stability	Lower	High	**High**
Flatness	Variable	Good	**Excellent**
Electrical insulation	Moderate	Low (silicon conducts)	**Excellent**
Cost at scale	Low	High	**Medium — falling**
Via density	Lower	High	**Very high**

Through-Glass Vias (TGVs)

Through-Glass Vias (TGVs) are tiny conductive channels — filled with metal (typically copper) — that pass vertically through a glass layer to connect chips stacked above and below:

1. A laser or chemical process **drills microscopic holes** through the glass
2. The holes are **filled with conductive metal**
3. Multiple chip layers can be **stacked and interconnected** through these vias
4. Signals travel **vertically** rather than being routed laterally on longer paths

This enables **heterogeneous integration** — combining different types of chips (CPU, GPU, memory, RF, analog) in a single compact package with minimal signal delay.

Why Glass Over Silicon Interposers?

- **Lower dielectric constant** — less signal loss at high frequencies (critical for AI and 5G)
- **Better CTE (coefficient of thermal expansion) match** — reduces stress at chip-substrate interface
- **Higher via density** — glass can achieve tighter via pitch than organic substrates
- **Optical transparency** — enables future photonic integration (optical data transmission within packages)
- **Lower fabrication cost** at scale compared to silicon interposers

THE BHUBANESWAR FACILITY

Specifications

PARAMETER	VALUE
Location	Bhubaneswar, Odisha
Technology	3D glass chip packaging with TGVs
Annual capacity	70,000 panels; 50 million units
First in	India — first such glass packaging facility
Target sectors	AI accelerators, defence electronics, telecom

Why Bhubaneswar?

Odisha has positioned itself as a technology manufacturing hub:

- **Proximity to port** — Paradip, Dhamra for component import/export
- **State semiconductor policy** — Odisha's incentive framework for electronics manufacturing
- **Land availability** — industrial corridors under development
- The facility also complements Odisha's broader marine and technology ambitions, including OMBRIC (Odisha Marine Biotechnology Research and Innovation Corridor)

INDIA SEMICONDUCTOR MISSION (ISM)

Overview

The **India Semiconductor Mission (ISM)** was launched in 2021 under the **Modified Programme for Semiconductors and Display Fab Ecosystem**:

PARAMETER	DETAIL
Total outlay	₹76,000 crore (~$9 billion)
Launched	December 2021
Nodal ministry	Ministry of Electronics and IT (MeitY)
Administered by	India Semiconductor Mission (ISM) — within MeitY
Scope	Fabs, ATMP (Assembly, Testing, Marking, Packaging), display fabs
Fiscal support	Up to 50% capital expenditure support for greenfield fabs

Key Approved Projects Under ISM

COMPANY	LOCATION	TECHNOLOGY	STATUS
Tata Electronics + PSMC	Dholera, Gujarat	28nm fab	Under construction
CG Power + Renesas + Stars Microelectronics	Sanand, Gujarat	ATMP/OSAT	Under development
Kaynes Semicon	Sanand, Gujarat	ATMP	Approved
ISMC (India Semiconductor Manufacturing Corporation)	Mysuru, Karnataka	Analog fab	Earlier approved; restructuring

The Bhubaneswar glass packaging facility adds **advanced packaging capacity** to India's semiconductor ecosystem — a segment where TSMC, Samsung, and Intel are investing globally.

ATMP vs. Fab — The Distinction

STAGE	DESCRIPTION	INDIA STATUS
Design	EDA tools, chip architecture	Strong (Qualcomm, Intel design centres in India)
Wafer Fabrication (Fab)	Manufacturing chips from silicon wafers	Under development (Dholera fab)
ATMP	Assembly, Testing, Marking, Packaging	Multiple projects approved
Advanced Packaging	2.5D/3D integration, glass substrates	**Bhubaneswar — India's first**

Advanced packaging sits between traditional ATMP and full-fab capability — and is strategically important because it determines the performance of final AI chips and defence systems.

BEYOND MOORE'S LAW — THE NEW PARADIGM

The semiconductor industry has shifted its roadmap from pure transistor scaling to a multi-dimensional approach:

DIMENSION	DESCRIPTION
More Moore	Continue shrinking transistors (3nm, 2nm, 1.4nm...)
More than Moore	Add functionality — integrating RF, MEMS, sensors with logic
Beyond CMOS	New transistor types — GaN, SiC, 2D materials
System-level integration	3D packaging, chiplets — the current dominant strategy

Heterogeneous integration — combining chips of different types, nodes, and technologies in one package — is why glass substrate packaging is strategically valuable. A single AI accelerator today may combine:

- An advanced logic die (3nm)
- High-bandwidth memory (HBM) stacks
- A networking chip
- All integrated in a 3D package with glass substrate

STRATEGIC IMPLICATIONS — AI AND DEFENCE

AI Accelerators

The global AI chip market is dominated by **NVIDIA's GPU clusters** using advanced CoWoS packaging (TSMC's Chip-on-Wafer-on-Substrate technology). As India builds AI computing infrastructure:

- Domestically packaged chips reduce **import dependency** for AI server components
- Glass substrate packaging directly targets the **high-performance computing segment**

Defence Electronics

India's **Make in India for Defence** requires indigenous chip packaging for:

- Radar signal processing chips
- Electronic warfare systems
- Secure communication hardware

Chips for defence applications cannot be sourced from potentially adversarial supply chains — making domestic 3D packaging capability a **national security asset**.

India's Semiconductor Imports

India currently imports **~$24-25 billion in semiconductors annually** — one of its largest import categories. ISM aims to achieve **~25-30% semiconductor self-sufficiency by 2030**.

UPSC RELEVANCE

PAPER	ANGLE
GS3 — S&T	Semiconductor technology, 3D packaging, Moore's Law, glass substrates, TGVs
GS3 — Economy	India Semiconductor Mission, import substitution, electronics manufacturing
GS2 — Governance	MeitY, ISM, Make in India, PLI scheme
Mains Keywords	ISM, 3D glass packaging, TGV, heterogeneous integration, Moore's Law, ATMP, chiplets, AI accelerators, Bhubaneswar

FACTS CORNER

- **Facility:** India’s first 3D glass chip packaging unit — Bhubaneswar, Odisha
- **Capacity:** 70,000 panels and 50 million units annually
- **Key innovation:** Through-glass vias (TGVs) — vertical conductive channels through glass for chip stacking
- **Glass advantage:** Lower signal loss, better thermal stability, higher via density than organic substrates
- **India Semiconductor Mission (ISM):** ₹76,000 crore outlay; MeitY; launched December 2021; up to 50% capex support
- **Dholera fab:** Tata Electronics + PSMC — 28nm fab; under construction; Gujarat
- **Moore’s Law:** Transistor density doubles every ~2 years (Gordon Moore, 1965); approaching physical limits
- **Heterogeneous integration:** Combining different chip types in one package — now the primary performance scaling strategy
- **India’s semiconductor imports:** ~$24-25 billion annually — one of largest import categories
- **ATMP:** Assembly, Testing, Marking, Packaging — India’s primary semiconductor entry point alongside packaging
- **CoWoS:** TSMC’s Chip-on-Wafer-on-Substrate — dominant AI chip packaging technology (used in NVIDIA GPUs)
- **HBM:** High-Bandwidth Memory — stacked DRAM used in AI accelerators; key beneficiary of 3D packaging

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