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**EDITORIAL ANALYSIS**

# India's Semiconductor Moment — From ATMP to Full-Stack Fabrication

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**SUBJECTS COVERED****ECONOMY****SCIENCE & TECH****GS PAPERS****GS3****CURATED & WRITTEN BY****Bharat Choudhary**

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# India's Semiconductor Moment — From ATMP to Full-Stack Fabrication

The Hindu

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GS3

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MAINS RELEVANCE:

GS Paper 3



## INTERVIEW ANGLE

*"Why can't India simply build its own semiconductor fabrication plant (fab) like Taiwan's TSMC, and what would be needed to get there?"*

## WHY IN NEWS

Micron Technology's inauguration of the world's largest semiconductor assembly clean room at Sanand, Gujarat, on February 28, 2026, marks India's first tangible step in the global semiconductor supply chain — but it also illuminates how far India remains from true semiconductor self-reliance.

## A LANDMARK, BUT NOT A REVOLUTION

Micron's Sanand facility is a genuine milestone. The world's largest single semiconductor assembly clean room on Indian soil, delivering DRAM modules for Dell — this is not a token gesture. It is \$2.7 billion of committed capital, 1,300 Indian engineers trained in Malaysia and Singapore, and an anchor for Gujarat's emerging electronics corridor.

But intellectual honesty requires acknowledging what Sanand is not. **Assembly, Testing, Marking and Packaging (ATMP)** is the last step in the semiconductor value chain, not the first. The silicon wafers being assembled at Sanand are fabricated at Micron's plants in Idaho, Singapore, and Japan. The intellectual property, the process nodes, the cutting-edge equipment — these are not in India.

## UNDERSTANDING THE SEMICONDUCTOR VALUE CHAIN

The semiconductor industry operates in distinct tiers of technological complexity and capital intensity:

**Tier 1 — Design:** Chip architecture (Intel, Qualcomm, Apple, ARM). India has significant presence here through engineers at global firms and through homegrown chip design companies (Saankhya Labs, InCore Semiconductors, Axiscades).

**Tier 2 — Fabrication (Fabs):** Where silicon wafers are processed into chips using photolithography. Requires extreme UV (EUV) machines costing \$200 million each (only ASML makes them). The most advanced fabs (TSMC, Samsung) invest \$20–30 billion per plant. This is where India is absent.

**Tier 3 — ATMP/OSAT:** Assembly and testing. Capital-intensive but less technologically demanding than fabs. This is where Micron Sanand operates.

India's semiconductor policy has focused heavily on Tier 3 — the right starting point, but not the destination.

## THE TATA DHOLERA GAMBIT

The more ambitious bet is the **Tata Electronics semiconductor fab** in Dholera, Gujarat, announced with TSMC as a technology partner. If realised, this would be India's first genuine front-end fab — processing wafers with lithography equipment.

However, the challenges are formidable. TSMC's global dominance rests on decades of accumulated process knowledge, a dense ecosystem of local suppliers, and the unique chemistry of Taiwan's engineering workforce. Moving that to India — even with technology transfer — means rebuilding an ecosystem from scratch.

The government has committed **50% capital subsidy** on fab investments under the India Semiconductor Mission. For a \$10 billion fab, that is \$5 billion in public money — a bet on a decades-long payoff. Whether that payoff materialises depends on sustained policy commitment beyond electoral cycles, something India's industrial policy has historically struggled to guarantee.

## THE TALENT QUESTION

India produces **1.5 million engineering graduates annually** — but semiconductor manufacturing requires not just engineers, but engineers trained in very specific disciplines: materials science, process engineering, device physics, yield management. These specialisations did not exist in India's educational ecosystem because there was no domestic semiconductor industry to absorb them.

Micron's model — recruiting fresh graduates and training them abroad — works for ATMP. It will not scale to fab operations, which require engineers who can debug lithography process windows and manage sub-nanometre dimensional control. This talent must be built at home, which requires dedicated university programmes, industry-sponsored research, and time.

**IIT Bombay's Nano Fabrication Facility** and a handful of other research institutions have fab-grade equipment for academic use. But bridging the gap from academic exposure to industrial-scale process engineering is a generational project.

## THE GEOPOLITICAL CASE FOR URGENCY

The strategic case for semiconductor self-reliance is unambiguous. The US-China technology war has weaponised chips — US export controls now restrict advanced semiconductor equipment to China. Taiwan, which produces ~90% of the world's most advanced chips, sits across a strait from a China that claims it as sovereign territory.

For India — which imports nearly \$24 billion in semiconductors annually — a Taiwan disruption scenario would be catastrophic for everything from smartphones to defence systems to railway signalling.

The Micron Sanand facility reduces this vulnerability at the margin. It does not eliminate it. Only a credible indigenous fab capability — years or decades away — would provide genuine strategic insulation.

## WHAT SUCCESS LOOKS LIKE

India's semiconductor strategy should be measured by three milestones:

**Short-term (by 2027):** Micron Sanand at 1 billion units/year; CG Power and Kaynes ATMP facilities operational; domestic demand for ATMP rising.

**Medium-term (by 2030):** Tata Dholera fab operational at mature process nodes (28nm or above); chip design exports growing; domestic chip design addressing defence electronics needs.

**Long-term (post-2030):** India capable of advanced node fabrication (sub-10nm) with indigenous EDA tools, process IP, and materials supply chain — true semiconductor sovereignty.

Sanand is the right beginning. The question is whether India's policy continuity, talent pipeline, and capital mobilisation can sustain the full journey.

### UPSC RELEVANCE

ATMP, ISM, MeitY, EUV lithography, TSMC, ASML, India Semiconductor Mission outlay.

### MAINS GS-3:

Semiconductor supply chain; strategic autonomy; technology policy; industrial development.

### INTERVIEW:

India's position in the global semiconductor value chain — strengths, gaps, and strategy.

## ★ FACTS CORNER — KNOWLEDGEPEDIA

### INDIA SEMICONDUCTOR MISSION (ISM):

Outlay: **₹76,000 crore (~\$10 billion)**; Ministry: **MeitY**

Capital subsidy: **50%** on approved project costs

Three schemes: Semiconductor Fabs, ATMP/OSAT, Compound Semiconductors

### GLOBAL SEMICONDUCTOR VALUE CHAIN:

Design: Qualcomm, Intel, Apple, ARM (India has design talent here)

EUV machines: Only **ASML** (Netherlands) makes them; cost **~\$200 million each**

Advanced fabs (TSMC, Samsung): **\$20–30 billion** per plant

TSMC: Produces **~90%** of world's most advanced chips (in Taiwan)

### INDIA SEMICONDUCTOR PROJECTS:

Micron (Sanand): ATMP, \$2.7 billion, **500,000 sq ft** clean room

Tata Electronics (Dholera): Front-end fab, TSMC technology partnership

CG Power + Renesas (Sanand): ATMP facility

Kaynes Semicon (Sanand): ATMP facility

### KEY NUMBERS:

India semiconductor imports: **~\$24 billion/year**

India engineering graduates: **~1.5 million/year**

Micron 2027 target: **~1 billion units/year**

IIT Bombay Nano Fabrication Facility: India's premier academic fab

### OTHER RELEVANT FACTS:

US CHIPS Act (2022): \$52 billion; EU Chips Act (2023): targets 20% global share by 2030

“China+1” strategy benefits India as companies diversify from China

India's chip design strengths: ARM, Qualcomm, Intel, Texas Instruments all have large India design centres

Sources: The Hindu, MeitY, PIB

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