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Chips and Choices — India's Semiconductor Ambitions and the DLI Scheme

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Chips and Choices — India's Semiconductor Ambitions and the DLI Scheme

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INTERVIEW ANGLE

"Can India realistically become a semiconductor manufacturing hub? What are the structural constraints and what is the government's strategy to overcome them?"

Semiconductors — the chips that power everything from smartphones to fighter jets — are the defining industrial battleground of the 21st century. The COVID-19 pandemic exposed how a shortage of chips worth a few dollars could shut down automobile factories worth billions. Geopolitical rivalry between the United States and China has transformed semiconductor supply chains into national security infrastructure. And India, having missed the first wave of semiconductor manufacturing, is now attempting — ambitiously and expensively — to build a domestic chip industry from near-zero. The Design Linked Incentive (DLI) Scheme is one pillar of this effort.

INDIA'S SEMICONDUCTOR GAP — THE CONTEXT

India consumes approximately $25 billion worth of semiconductors annually (2024 estimate) and imports virtually all of them. This import dependence creates three distinct vulnerabilities:

Supply chain vulnerability: The pandemic revealed that just-in-time global chip supply chains can collapse rapidly. India's electronics manufacturing sector — targeting $300 billion by 2026 under the PLI scheme — depends entirely on imported chips for final assembly.

Strategic vulnerability: Advanced semiconductors in defence electronics, space systems, and telecommunications infrastructure come from US, Taiwan, and South Korean foundries. In a crisis, access cannot be guaranteed. China's increasing pressure on Taiwan makes this particularly acute.

Economic value capture gap: India assembles electronics but captures only the low-value-add portion of the supply chain. The highest value in electronics — chip design and fabrication — happens elsewhere.

THE GLOBAL SEMICONDUCTOR LANDSCAPE

Understanding India's ambitions requires understanding the industry's extraordinary complexity:

The chokepoints: TSMC (Taiwan) and Samsung (South Korea) manufacture ~90% of the world's most advanced chips (below 7nm). ASML (Netherlands) holds a near-monopoly on EUV lithography machines required for leading-edge fabrication. NVIDIA and AMD design the GPUs powering the AI revolution using fab-less model (design in USA, manufacture in Taiwan).

The investment scale: A leading-edge semiconductor fab (fabrication plant) costs $15-25 billion to build and requires 3-5 years to construct. Operating costs are enormous. TSMC's Arizona fab — being built with $40 billion in US government support — illustrates the required scale of public subsidy.

The talent requirement: Semiconductor design and fabrication require highly specialised engineers. The US has ~340,000 semiconductor workers; Taiwan has built its workforce over 50 years of deliberate industrial policy.

The China factor: US export controls (CHIPS and Science Act 2022 + subsequent restrictions) are attempting to freeze China at the ~7nm node, preventing it from accessing advanced chips for AI and military applications. This has created demand for non-Chinese alternative supply chains — an opportunity India is trying to capture.

INDIA'S SEMICON INDIA PROGRAMME — ARCHITECTURE

The Government of India launched the **India Semiconductor Mission (ISM)** in December 2021 under a three-pronged strategy:

Pillar 1 — Fabrication (Fabs): 50% fiscal support for setting up semiconductor fabrication plants in India. The first approval came in 2024: Tata Electronics (partnering with PSMC, Taiwan) for a fab in Dholera, Gujarat (28nm technology; Rs 91,000 crore investment); and Micron Technology (USA) for an assembly and test facility in Sanand, Gujarat.

Pillar 2 — ATMP/OSAT: 50% fiscal support for Assembly, Testing, Marking and Packaging (ATMP) and Outsourced Semiconductor Assembly and Test (OSAT) facilities. These are the lower-complexity steps in the chip supply chain. CG Power (with Renesas, Japan) received approval for a facility in Sanand.

Pillar 3 — Design (DLI Scheme): 50% support for chip design startups and companies. This is the most scalable pillar because chip design is software-intensive and can be done with far less capital than fabrication.

THE DLI SCHEME — DESIGN LINKED INCENTIVE

The **Design Linked Incentive (DLI) Scheme** is administered by **MeitY (Ministry of Electronics and Information Technology)**. Key parameters:

> **Financial support:** Up to 50% of eligible expenditure for chip design companies, over 5 years
>
> **Deployment incentive:** 6% to 4% incentive on net sales of semiconductor chips designed in India, over 5 years

Target: 20 domestic semiconductor design companies with a turnover of Rs 1,500 crore each within 5 years

Capital equipment: Support for design tools (EDA software — which costs millions of dollars per seat per year) reduces the entry barrier for Indian startups

Eligibility: Indian companies designing semiconductor or embedded hardware products

Why design first? India has a legitimate competitive advantage in chip design: a large pool of engineering talent (IITs, NITs), strong mathematics education, and an existing software services industry with relevant skills. Chip design using tools like VLSI (Very Large Scale Integration), EDA (Electronic Design Automation), and FPGA (Field Programmable Gate Array) is an extension of software capabilities that India already has.

Companies like **Saankhya Labs** (ISRO-linked satellite receiver chips), **Tessolve**, **Signalchip**, and numerous VLSI design startups are building India's chip design ecosystem. Globally, Indian engineers already lead chip design teams at Intel, Qualcomm, ARM, and NVIDIA — the DLI aims to anchor this talent in India.

THE TALENT AND ECOSYSTEM CHALLENGE

Despite the policy ambition, India faces structural gaps:

The EDA tool problem: Electronic Design Automation software (Synopsys, Cadence, Mentor Graphics — all US companies) is the essential tooling for chip design. Individual licenses cost $1-5 million annually. DLI subsidies help, but the dependence on US-controlled EDA tools means chip design is not truly "India's" in a strategic sense.

The IP stack: Modern chips are not designed entirely from scratch. They use IP blocks (ARM architecture for processors, for instance). India lacks a domestic IP foundation, meaning every "Indian chip" still depends on licensed foreign IP.

The fabless paradox: DLI encourages design. But design without domestic fabrication means Indian-designed chips must still be manufactured in Taiwan or South Korea. This is not strategically sovereign — it merely shifts one chokepoint (import dependence) while maintaining another.

The talent pipeline: India graduates ~1.5 million engineers annually, but the specialised semiconductor curriculum is thin. IISc Bangalore, IIT Bombay, and IIT Madras have strong research programmes, but industry-ready talent for fabrication is scarce. VLSI education is improving but still inadequate in volume.

THE COMPARISON WITH CHINA'S CHIPS POLICY

China's response to US export controls is instructive. Despite being blocked from advanced chips, China has:

Poured $150+ billion into its domestic semiconductor industry since 2014 via the National IC Fund (Guiding Fund)

Achieved domestically competitive chips at the 28nm node (SMIC, China)

Developed proprietary EDA tools (Empyrean Technology)

Built massive DRAM and NAND flash manufacturing capacity (CXMT, YMTC)

India is not facing the same pressure China is — nor does it have China's industrial capacity, authoritarian resource mobilisation, or 50-year lead time. But the lesson from China is that semiconductor self-sufficiency requires sustained multi-decade commitment at a scale that India has not yet demonstrated.

WHAT SUCCESS WOULD LOOK LIKE

A realistic 10-year benchmark for India's semiconductor mission:

3-4 ATMP/OSAT facilities operational (achievable — lower barrier than fabs)

1-2 mature-node fabs (28nm-90nm) operational at scale (Dholera + one more)

50+ DLI-supported design companies generating $1 billion+ in chip design revenue

Indian engineers developing proprietary chip IP in defence (DRDO), space (ISRO), and telecom (5G/6G chips for BharatNet)

No leading-edge (below 7nm) capability — that remains a 20-30 year goal

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INDIA SEMICONDUCTOR MISSION — KEY NUMBERS:

Total outlay: Rs 76,000 crore (~$9 billion) for the India Semiconductor Mission programme

Fab incentive: 50% fiscal support for setting up fabs

ATMP/OSAT incentive: 50% fiscal support

DLI Scheme: 50% of eligible expenditure; 6-4% incentive on net sales over 5 years

DLI target: 20 domestic semiconductor design companies with Rs 1,500 crore turnover each in 5 years

Administering body: MeitY (Ministry of Electronics and Information Technology)

APPROVED SEMICONDUCTOR PROJECTS IN INDIA (2024):

Tata Electronics + PSMC (Taiwan): Fab at Dholera, Gujarat; 28nm technology; Rs 91,000 crore

Micron Technology (USA): ATMP/OSAT at Sanand, Gujarat; Rs 22,516 crore investment

CG Power + Renesas (Japan) + Stars Microelectronics (Thailand): ATMP at Sanand, Gujarat

Kaynes Semicon: ATMP at Sanand, Gujarat

GLOBAL SEMICONDUCTOR LANDSCAPE:

TSMC (Taiwan Semiconductor Manufacturing Company): world's largest foundry; 90%+ of sub-7nm chips

ASML (Netherlands): sole supplier of EUV (Extreme Ultraviolet) lithography machines — required for leading-edge chips; each machine: ~$350 million

US CHIPS and Science Act (2022): $52 billion for domestic US semiconductor manufacturing; restricts advanced chip exports to China

China's CXMT: DRAM producer; SMIC: largest Chinese foundry (stuck at ~7nm due to US restrictions)

INDIA ELECTRONICS ECOSYSTEM:

India's semiconductor import: ~$25 billion annually (2024)

PLI Scheme for IT Hardware: Rs 17,000 crore; targets $300 billion electronics manufacturing by 2026

India's current electronics manufacturing: ~$100 billion (2024)

iPhone manufacturing in India: Apple + Foxconn (Tamil Nadu) + Wistron/Tata Electronics (Karnataka)

KEY TERMS:

Fab (Fabrication Plant): where silicon wafers are etched with chip circuits; requires Class 10 cleanrooms

ATMP (Assembly, Testing, Marking and Packaging): lower-complexity chip packaging step; less capital-intensive than fab

EDA (Electronic Design Automation): software tools for chip design; dominated by US companies (Synopsys, Cadence)

VLSI (Very Large Scale Integration): chip design with millions+ transistors on one die

Fabless model: companies that design chips but outsource fabrication (e.g., Qualcomm, NVIDIA, Apple)

Leading-edge node: below 7nm (currently 3nm and 2nm); advanced AI and mobile chips

Mature node: 28nm-90nm; sufficient for automotive, industrial, defence electronics — India's near-term goal

OTHER RELEVANT FACTS:

DSIR (mentioned in Jan 6 news): Department of Scientific and Industrial Research; manages PRISM for startups; 42nd Foundation Day, 2026

National Policy on Electronics 2019: targets $400 billion electronics manufacturing and 1 billion mobile handsets by 2025

> ICAT (International Centre for Automotive Technology): designs automotive semiconductor chips for Indian OEMs
>
> DRDO's semiconductor work: developing custom chips for missile guidance, electronic warfare under self-reliance programmes

Sources: Mint, MeitY, PIB, India Semiconductor Mission

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